Formula 1

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Formula 2

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Formula 3

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Detailed Explanation

Near-field probe scanning is a cornerstone technique in pre-compliance EMI debugging, leveraging the fact that electromagnetic fields decay rapidly ($1/r^2$ for reactive near-field, $1/r$ for radiating near-field) within distances less than ?/2?—typically millimeters at MHz–GHz frequencies. The protocol begins with environmental preparation: shielding the setup from ambient RF, grounding the scan stage and DUT properly, and selecting appropriate probe types (e.g., sub-5 mm loop probes for H-field localization of current loops; short monopole or dipole probes for E-field mapping of high dv/dt nodes). A structured scan plan follows—defining grid resolution (e.g., 1–2 mm steps), probe height (0.5–3 mm above copper), bandwidth settings (RBW ? 10 kHz for narrowband, ?100 kHz for broadband), and dynamic range optimization—to ensure repeatability and sensitivity without saturation. Data acquisition is synchronized with stimulus conditions (e.g., toggling specific peripherals or clock domains), enabling differential (‘on/off’) scans that suppress common-mode background noise. Post-scan analysis uses amplitude contour maps, frequency-domain spectral overlays, and spatial correlation with layout data (e.g., matching hotspots to gate drivers, DC-DC inductors, or unterminated traces) to formulate and validate hypotheses—e.g., whether a hotspot stems from a ground bounce resonance or an unintentional antenna formed by a split plane. Crucially, the flowchart enforces iterative refinement: each identified suspect is mitigated (e.g., via ferrite beads, local decoupling, or trace routing changes), followed by re-scanning to verify suppression and avoid masking secondary issues.

Key Components

#	Component
1	Near-field probe selection (H-field vs. E-field)
2	Controlled scan parameters (step size, height, RBW, detector mode)
3	Differential measurement methodology (stimulus-aware on/off comparison)

Applications

#	Application
1	Pre-compliance EMI root-cause analysis during PCB bring-up
2	Validation of layout fixes before formal CISPR/EN 55032 testing
3	Design validation for high-speed digital interfaces (PCIe, USB, DDR) and switch-mode power supplies

Related Concepts

#	Concept
1	Electromagnetic Compatibility (EMC) Design
2	Return Path Integrity
3	PCB Stackup Optimization
4	Common-Mode vs. Differential-Mode Emissions

Tags

> EMI debugging, near-field scanning, PCB compliance, EMC engineering, pre-compliance testing